ABSTRACT

Structure and method for fabrication of a leadless chip carrier have been disclosed. A disclosed embodiment comprises a substrate having a top surface for receiving a semiconductor die. The disclosed embodiment also comprises a printed circuit board attached to a bottom surface of the substrate. The disclosed embodiment further comprises at least one via in the substrate, which provides an electrical connection between a signal bond pad of the semiconductor die and the printed circuit board. The at least one via also electrically connects a substrate bond pad and the printed circuit board. The substrate bond pad is further connected to the signal bond pad of the semiconductor die by a signal bonding wire. The at least one via further provides an electrical connection between the signal bond pad of the semiconductor die and a land that is electrically connected to the printed circuit board.